<u>What is claimed is:</u>

1.   A   synchronous   semiconductor   memory   device,
comprising:

5   a clock synchronization means for synchronizing a data
output with an external clock; and

a clock tree on/off control means for delaying an enable
timing of a RAS idle signal for a predetermined time after a
row inactive instruction is supplied to selectively turning

10   on/off a clock tree of the clock synchronization means in
response to the RAS idle signal.

2.   The   synchronous   semiconductor   memory   device   as
recited in claim 1, wherein the clock synchronization means

15   includes a delay locked loop.

3.   The   synchronous   semiconductor   memory   device   as
recited in claim 1, wherein the clock synchronization means
includes a phase locked loop.

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4.   The   synchronous   semiconductor   memory   device   as
recited in claim 1, wherein a clock tree on/off control means
includes:

a   first   edge   triggered   pulse   generating   means   for

25   generating a first edge triggered pulse by receiving a RAS
idle signal;

a clock buffering means for buffering a clock signal

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having the same period with the external clock in response to the RAS idle signal and a feedback clock tree control signal;

a clock period configuration means for deciding a period as same as a clock period of a predetermined output signal from the clock buffering means in response to the RAS idle signal;

a second edge triggered pulse generating means for generating a second edge triggered pulse by receiving an output signal of the clock period configuration means; and

a latching means for receiving both output signals of the first edged triggered generating means as a set signal and the second edged triggered generating means as a reset signal.

5. The synchronous semiconductor memory device as recited in claim 4, wherein the clock period configuration means includes a clock divider.

6. The synchronous semiconductor memory device of claim 4, wherein the clock period configuration means includes multi-cascaded flip-flops.

7. The synchronous semiconductor memory device of claim 4, wherein the clock period configuration means includes a counter.

8. The synchronous semiconductor memory device of claim 5, wherein the clock divider includes:

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a plurality of flip-flops having a reset terminal for receiving the RAS idle signal and a clock terminal for receiving an inverse signal of itself output; and

a plurality of inverters connected between a output terminal and a input terminal of each inverter for delivering a converted output signal to the input terminal,

wherein each flip-flops is cascade-connected to each other by receiving the output of a prior flip-flop at a clock terminal.

9. The synchronous semiconductor memory device of claim 4, the first edge triggered pulse generating means generates the first edge triggered pulse by triggering rising or falling edges of the RAS idle signal.

10. The synchronous semiconductor memory device of claim 4, wherein the clock buffering means includes:

a NAND gate receiving the RAS idle signal, the feedback clock tree control signal, and a clock signal being same to the external clock; and

a plurality of inverters for buffering an output of the NAND gate.

11. The synchronous semiconductor memory device of claim 4, wherein the latching means is initialized by a power-up signal.

12. The synchronous semiconductor memory device of claim 11, wherein the latching means includes a cross-coupled NAND latch

5   13. The synchronous semiconductor memory device of claim 12, wherein the cross coupled NAND latch includes:

a first NAND gate receiving an output of the first edge triggered pulse generating means and an output of a second NAND gate; and

10   the second NAND gate receiving the power-up signal, an output of the second edge triggered pulse generating means and an output of the first NAND gate.

14. The synchronous semiconductor memory device of claim 15   4, wherein the clock synchronization means includes a delay locked loop.

15. The synchronous semiconductor memory device of claim 4, wherein the clock synchronization means includes a phase 20   locked loop.